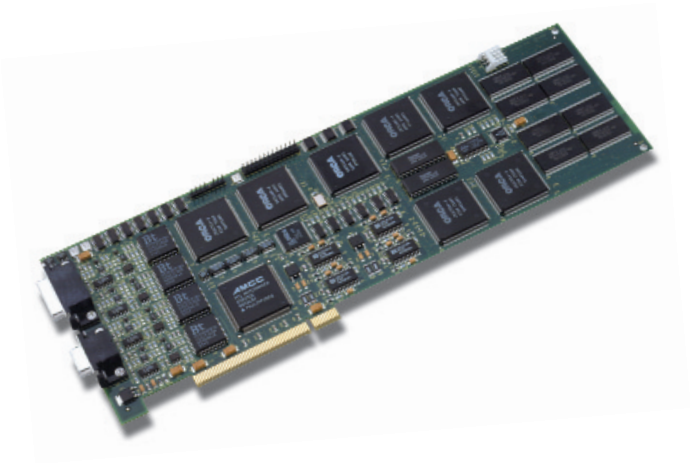
CORECO IMAGING

IC-ASYNC

High-Speed, Asynchronous Image Capture
for Multipoint Applications



VIDEO FORMATS

- Supports independent asynchronous acquisitions from up to 4 cameras
- Supports non-standard area scan cameras up to 1K x 1K; variable scan
- Supports up to 2 dual-tap asynchronous camera inputs

FEATURES & BENEFITS

- On-board 1MB frame buffer for each of the 4 channels.
- DMA bus master transfers images to host memory in less than 4 ms
- Non-destructive overlay using compatible SVGA adapters
- Hardware circuitry automatically de-interlaces images during acquisition
- Supports trigger, strobe, and frame reset for applications demanding highly responsive asynchronous image capture
- Multiple frame ping-pong source and destination capabilities for simultaneous acquisition and transfer of images to host memory
- On-board 16-bit digital I/O allows for easy connection to industrial I/O peripherals

APPLICATIONS

- High-speed consumer package, can/bottle and pharmaceutical inspection
- Multiple independent production lines
- Multi-point integrated circuit device inspection
- High speed Tandem batch inspection

SOFTWARE

- Camera Configurator®—Windows utility for easy board and camera set-up
- ITEX® Driver and board function libraries
- MVTools® Machine vision, image processing and image analysis libraries

OVERVIEW

IC-ASYNC represents breakthrough technology that, for the first time, integrates 4 independent, asynchronous frame grabbers on one full size PCI-bus card. With the ability to acquire up to 4 camera channels asynchronously, the IC-ASYNC can handle high speed applications that traditionally could only be solved using expensive and complicated vision processors.

Each of the four channels on the IC-ASYNC can acquire images independently and asynchronously. Every channel has its own 1MB frame buffer. Video input can be composite, variable scan, progressive scan, or VGA. Independent external trigger, frame reset, strobe, sync, timebase settings, AOI settings, and input conditioning circuitry is provided for each channel.

Each frame buffer acquires image data independently based on timing from its associated camera input channel. A de-interlacing feature allows consecutive fields to be merged during acquisition. Multiple frame modes allow up to 8 images to be consecutively acquired into the frame buffer. Ping-Pong bus master mode allows consecutive acquisition and transfer of images with no lost frames guaranteed! A sub-sample mode allows for decimation of the incoming video data (x2, X and Y) for resizing images on-the-fly.

The IC-ASYNC incorporates a state-of-the-art bus master controller (BMC) that autonomously monitors images as they are being acquired into each of 4 frame buffers and transfers the image data

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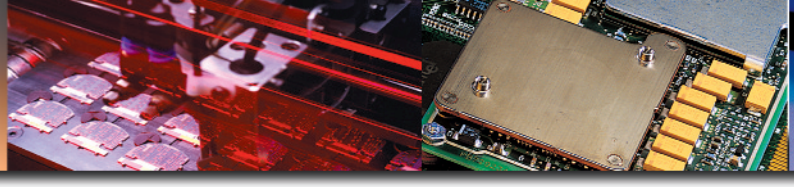
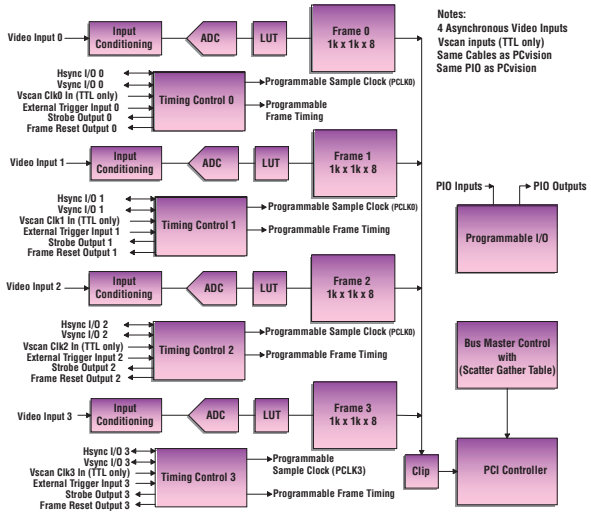


to host memory (interrupt based). The host CPU is free to process data during bus master transfers rather than controlling each individual transfer operation. The BMC provides multiple frame ping-pong source and destination capabilities which enables continuous real-time processing of each image. The BMC uses a programmable scatter gather table that eliminates the need for the host to monitor bus master transfers.

HIGH SPEED DATA TRANSFERS

IC-ASYNC provides a high-speed 32-bit PCI-bus interface that can be configured as a DMA bus master or slave. In bus master mode, special circuitry automatically de-interlaces images "on the fly," allowing data to be DMA transferred a frame at a time directly into a destination in memory within the system. The IC-ASYNC reduces CPU overhead and sustains transfer rates in excess of 120MB/s to the PCI-bus, as compared to other frame grabbers that constantly demand host CPU cycles. As a result, images can be transferred to host memory in a fraction of the time it takes to acquire them. By minimizing PCI-bus transfer time, more bandwidth is available for other system functions.

IC-ASYNC Block Diagram



COMPREHENSIVE VISION SOFTWARE TOOLS

To simplify and speed set-up time, Coreco Imaging's Camera Configurator® provides a Windows based point-and-click utility for configuring of all camera and interface board parameters.

ITEX® software provides users with a simple sophisticated API that provides superior control. Full multi-threaded interrupt support is provided for maximum efficiency. Easy to use high level calls allow efficient bus mastering, display, and overlay capabilities.

MVTools®/SMART, the core algorithm library from Sherlock™, is a complete set of C/C++ based software tools for vision professionals developing machine vision systems. Designed for speed, ease of use, and precision, MVTools offers a comprehensive library of vision development tools that significantly reduces time-to-market.

SPECIFICATIONS

SENSOR INTERFACE:
- Four independent analog video inputs, AC coupled & terminated to 75 Ohms
- Monochrome "standard" video camera and sources: RS-170, CCIR, VGA etc,. accepts composite video or timing (HS, VS, PCLK); or driven with external timing (HSYNC, VSYNC, VRESET)
- 2 dual-tap asynchronous camera inputs
- Programmable Timebase Generator; programmable resolution to 1024 x 1024 interlaced or non-interlaced. Outputs horizontal, vertical and reset timing to camera
- Programmable PLL (Phase-Locked Loop) Video Digitizer
- 20 MHz Monotonic 8-bit flash ADC; Input pixel rates to 20 MHz Video

VIDEO MEMORY
- 4 independent 1MB frame buffers ON-BOARD DIGITAL I/O
- 16 bits: 8 bits in; 8 bits out
- Input Latching

VIDEO SIGNAL CONDITIONING
- Programmable gain adjust - positive ADC reference (full-scale) from 0 to +2 Volts in 64 steps
- Programmable offset - negative ADC reference (zero) software programmable from 0 to +1.2 Volts in 64 steps
- Look-Up Table - 8 in - 8 out following ADC
- DC Restoration - programmable clamp pulse
- Input gain - software selectable: 1.0x or 1.5x
- Low-pass filter 6.0 MHz fixed

EXTERNAL TRIGGER, STROBE CONTROL, AND FRAME RESET
- External Trigger input per camera; synchronizes acquisition to external events. Falling edge trigger - minimum input pulse width 50 nsec
- Frame Reset Mode: external trigger initiates camera frame reset, strobe, and image acquisition for immediate capture of moving objects
- Trigger on Frame Mode: strobing and image acquisition are synchronized with the video signal
- Strobe outputs per camera with programmable polarity; 120-msec nominal duration
- Programmable position of strobe relative to camera timing
- Programmable frame reset delay 1 to 511 lines (increments of one line)
- Acquire on next field

VIDEO WINDOW GENERATOR
- Allows selection of video window within video signal
- Horizontal offset programmable 0 to1023 pixels (one increments)
- Horizontal size programmable from 4 to 1024 pixels (increments of four)
- Vertical offset programmable 0 to 1023 lines (one increments)
- Vertical size programmable 1 to 1024 lines (one increments)

INTERRUPTS
- Host interrupt on occurrence of strobe, trigger, VB or acquisition

HARDWARE COLOR DOT CLIPPING
- Image data can be "clipped" during bus master to a Windows display device to eliminate any conflicts with Windows reserved colors.

ON-BOARD DECIMATION
- Image reduction on acquisition by factors of 2

DISPLAY - WINDOWS:
- Provides Non-destructive Overlay
- A DirectX compatible SVGA adapter required for real-time display

AUTOMATIC DOUBLE BUFFERED FULL FRAME ACQUISITION
- Hardware controlled "ping-pong" acquisition into image memory, provides most efficient acquisition and bus-master synchronization possible

BUS REQUIREMENTS:
- 32-bit PCI slot
- 1.3 A @ +5 Volts
- 0.2 A @ + 12 Volts
- Full slot PCI card

POWER OUTPUT
- 500 mA @ +12 Volts/camera
- 500 mA @ +5 Volts to digital I/O (2 A total)

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